REMARKS

In view of the following discussion, the Applicants submit that none of the claims now pending in the application is anticipated under the provisions of 35 U.S.C. § 102 or is rejected under the judicially created doctrine of double patenting. Thus, the Applicants believe that all of these claims are now in allowable form.

**I. REJECTION OF CLAIMS 22-24, 27-34, AND 37-38 UNDER THE JUDICIALLY CREATED DOCTRINE OF DOUBLE PATENTING**

The Examiner rejected claims 22-24, 27-34, and 37-38 in Paragraph 3 of the Final Office Action under the judicially created doctrine of double patenting. Specifically, claims 22-24, 27-34, and 37-38 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-13 of US Patent No. 6,023,296.

Responsive to the Examiner, Applicants provisionally agree to file a terminal disclaimer to overcome this nonstatutory double patenting rejection. Specifically, Applicants will file the terminal disclaimer if and when all the present objections and rejections have been resolved.

**II. REJECTION OF CLAIMS 22-38 UNDER 35 U.S.C. § 102**

The Examiner in Paragraphs 2 and 4 of the Final Office Action again rejected claims 22-38 as being anticipated by the Eleftheriadis *et al.* patent (United States patent 6,055,330 issued April 25, 2000). The rejection is respectfully traversed.

Eleftheriadis *et al.* teaches a method and apparatus for performing image compression and segmentation by using 3-D depth information. Namely, Eleftheriadis *et al*'s device is able to exploit depth information to assist in the compression and segmentation of images. (See Eleftheriadis *et al*, Abstract)

The Examiner's attention is directed to the fact that Eleftheriadis *et al* fails to disclose Applicants' concept of allocating a target frame bit rate among the at least one object, wherein said allocating step comprises the step of allocating said target frame bit rate in accordance with a target object bit rate for the at least one object. Specifically, Applicants' claims 22, 29 and 32 positively recite:

> 22. A method for allocating bits to encode each frame of an image sequence, each of said frame having at least one object, said method comprising the steps of:
>
> (a) determining a target frame bit rate for the frame; and

(b) allocating said target frame bit rate among the at least one object, wherein said allocating step comprises the step of allocating said target frame bit rate in accordance with a target object bit rate for the at least one object. (emphasis added)

29. Apparatus for encoding each frame of an image sequence, said frame having at least one object, said apparatus comprising:

a motion compensator for generating a predicted image of a current frame;

a transform module for applying a transformation to a difference signal between the current frame and said predicted image, where said transformation produces a plurality of coefficients;

a quantizer for quantizing said plurality of coefficients with at least one quantizer scale; and

a controller for selectively adjusting said at least one quantizer scale for a current frame in response to a target object bit rate for the at least one object, wherein said target object bit rate is derived from a target frame bit rate. (emphasis added)

32. A computer-readable medium having stored thereon a plurality of instructions, the plurality of instructions including instructions which, when executed by a processor, cause the processor to perform the steps comprising of:

(a) determining a target frame bit rate for the frame; and

(b) allocating said target frame bit rate among the at least one object, wherein said allocating step comprises the step of allocating said target frame bit rate in accordance with a target object bit rate for the at least one object. (emphasis added)

In brief, Applicants disclose the novel concept of computing a target object bit rate for each object and then allocating a target frame bit rate among the objects in accordance with their computed target object bit rates. This concept is absent in the Eleftheriadis *et al* patent.

Specifically, the Examiner again cited Column 11, line 53 to Column 12, line 32 in the Eleftheriadis *et al.* patent as disclosing this concept. Specifically, the Examiner alleged that "R is the frame bit rate, or target frame bit rate". However, a close reading of the cited section in the Eleftheriadis *et al* patent revealed that there is **no** disclosure as to the computation of a target frame bit rate that is then allocated among the objects in accordance with the objects' target bit rates. Instead, Eleftheriadis *et al.* states that:

"In accordance with that technique, each object is associated with a particular target average bit rate $R_i$, i=1, . . . , n-1, except for the background (object n). In order to maintain the given total average rate R necessary to prevent buffer overflow, the **background rate** is determined according to the formula:

$\sum_{i=0}^{n} \alpha_i R_i = R$ where $\alpha_i$ is the proportion (from 0.0 to 1.0) of the pixels in the frame that belong to object i. (Emphasis added, See, Eleftheriadis, Column 11, line 67 to Column 12, line 10)

Thus, Eleftheriadis *et al.* is simply disclosing an allocation approach where the average rate R necessary to prevent buffer overflow is used to compute the **background rate**. This is a clear teaching of Eleftheriadis *et al.*'s equation (4) and it does not require any further interpretation.

Eleftheriadis *et al.* also defines "R is the average output bit rate to be maintained by the buffer 1020". (See Eleftheriadis *et al.*, Column 13, lines 31-32). In other words, R represents a measure of the physical buffer "fullness" and it is **not** a "target frame bit rate" as claimed by the Applicants. Namely, Eleftheriadis *et al.*'s teaching of using the average output bit rate of a physical buffer to compute a background rate would not anticipate Applicants' invention that recites the novel concept of computing a target object bit rate for each object and then allocating a target frame bit rate among the objects in accordance with their computed target object bit rates.

Another clear indication is that Eleftheriadis *et al.* states that "referring again to FIG. 10, the rates $R_i$ are used in a buffer regulation process that uses a technique of buffer rate and buffer size modulation". (See Eleftheriadis *et al.*, Column 12, lines 40-42) It is absolutely clear that the object rate of Eleftheriadis *et al.* is premised on the buffer fullness and not based on a target frame rate.

In the Final Office Action, the Examiner reasoned that "any bit rate utilized to maintain buffer fullness, and prevent underflow can be considered a target bit rate as claimed by the Applicant". Applicants respectfully disagree.

Applicants specifically recite "a target **frame** bit rate" and not a general "target bit rate" as alleged by the Examiner. Generally, the buffer fullness is intended to operate with a transmission channel with a constant transmission rate. Thus, it is generally necessary to monitor the fullness of the buffer to avoid overflow and underflow conditions. Aside from this general understanding, it is improper to then simply extrapolate the teaching of the buffer fullness to the determination of a target frame bit rate. For example, if the buffer is too full, the encoder may simply drop a frame, change the coding mode of a frame, change the frame type, change the quantizer scale of a frame, change the quantizer scale of a slice, change the quantizer scale of a macroblock, change the block size, and so on. None of these possible solutions requires the determination of a target frame bit rate. The number of possible solutions

is endless in responding to buffer fullness conditions and involves numerous image processing fields. Is the Examiner indicating that Eleftheriadis *et al.*'s simple teaching of monitoring buffer fullness now anticipates all possible inventions relating to rate control, motion estimation, motion compensation, mode decision, frame type selection, block size selection and so on. The Examiner's interpretation is simply too broad.

It is respectfully requested that the Examiner reconsiders his position that R as defined by Eleftheriadis *et al.* can be interpreted to be a target frame rate as positively claimed by the Applicants. There is simply no support in Eleftheriadis *et al.* for this interpretation.

As such, claims 22, 29 and 32 are not anticipated by Eleftheriadis *et al.* and satisfy the requirements of 35 U.S.C. § 102. Claims 23-28, 30 and 33-38 depend, either directly or indirectly, from claims 22, 29 and 32 and recite additional features therefor. Since Eleftheriadis *et al.* fails to anticipate Applicants' invention as recited in Applicants' independent claims 22, 29 and 32, dependent claims 23-28, 30 and 33-38 are also not anticipated under 35 U.S.C. § 102 and are allowable for the same reason noted above.

## Conclusion

Thus, the Applicants submit that none of the claims, presently in the application, is anticipated under the provisions of 35 U.S.C. § 102. Consequently, the Applicants believe that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of the present adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Mr. Kin-Wah Tong, Esq. at (732) 530-9404 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

RECEIVED
CENTRAL FAX CENTER
SEP 08 2003

Respectfully submitted,

9/6/03

Kin-Wah Tong, Attorney
Reg. No. 39,400
(732) 530-9404

Moser, Patterson & Sheridan, LLP
Attorneys at Law
595 Shrewsbury Ave.
Shrewsbury, NJ 07702

OFFICIAL



Received from < 732 530 9808 > at 9/6/03 5:08:03 PM [Eastern Daylight Time]